Figure 1

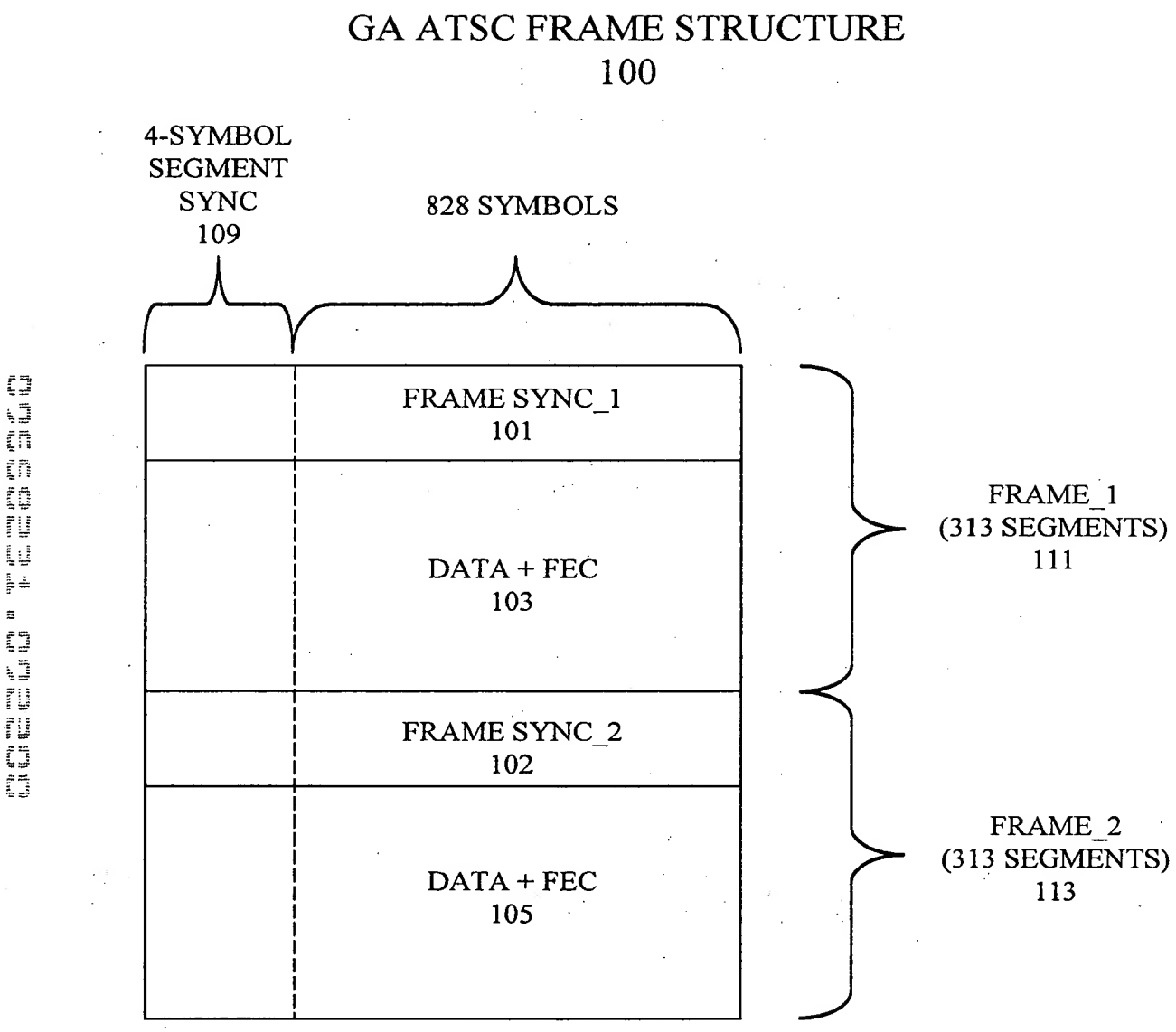

GA ATSC FRAME STRUCTURE
100
4-SYMBOL
SEGMENT
SYNC
109
828 SYMBOLS
FRAME SYNC_1
101
DATA + FEC
103
FRAME SYNC_2
102
DATA + FEC
105
FRAME_1
(313 SEGMENTS)
111
FRAME_2
(313 SEGMENTS)
113

Figure 2

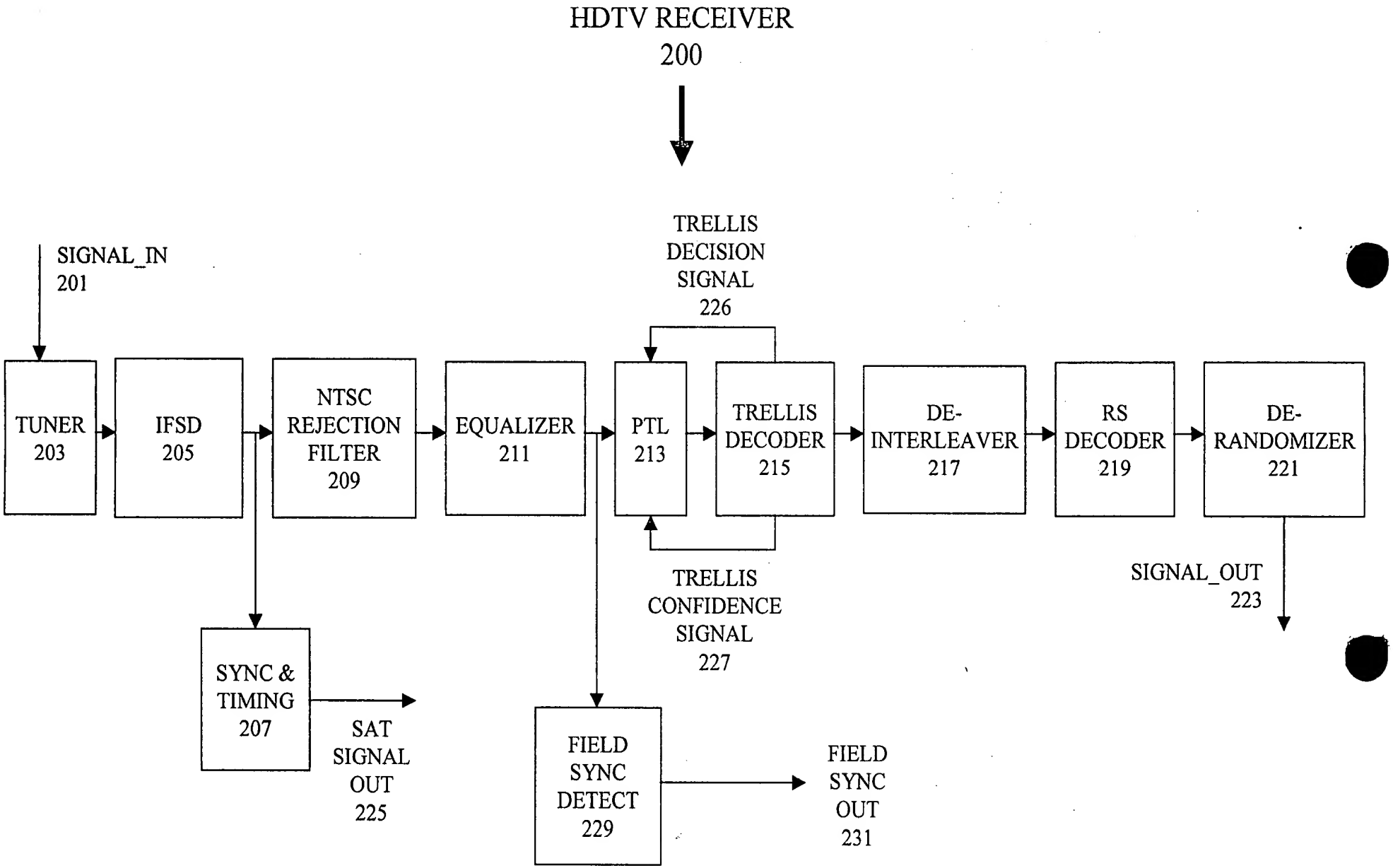

HDTV RECEIVER
200
SIGNAL_IN
201
TRELLIS
DECISION
SIGNAL
226
TUNER
203
IFSD
205
NTSC
REJECTION
FILTER
209
EQUALIZER
211
PTL
213
TRELLIS
DECODER
215
DE-
INTERLEAVER
217
RS
DECODER
219
DE-
RANDOMIZER
221
SIGNAL_OUT
223
TRELLIS
CONFIDENCE
SIGNAL
227
SYNC &
TIMING
207
SAT
SIGNAL
OUT
225
FIELD
SYNC
DETECT
229
FIELD
SYNC
OUT
231

Figure 3

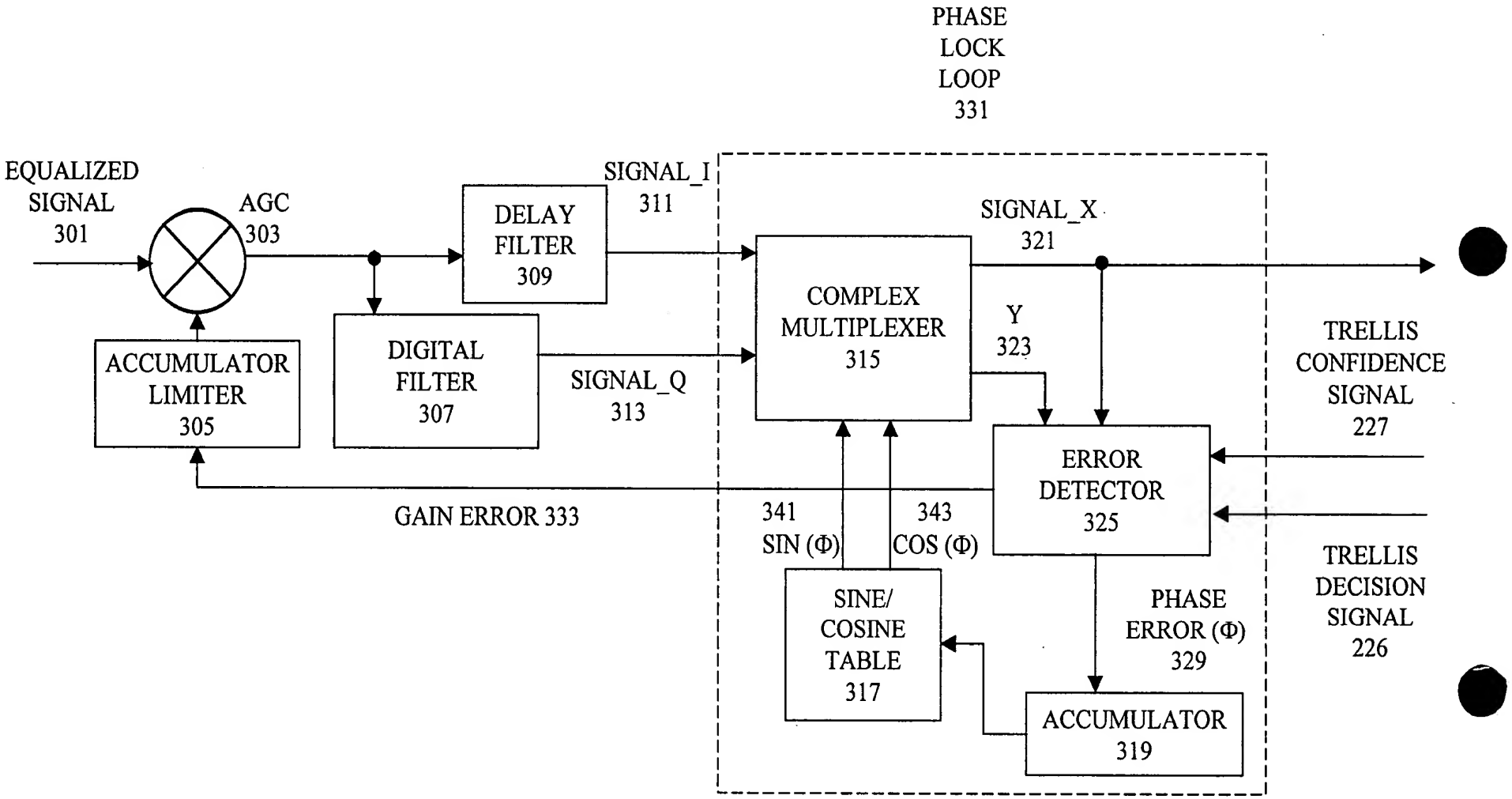

PHASE
LOCK
LOOP
331
EQUALIZED
SIGNAL
301
AGC
303
DELAY
FILTER
309
SIGNAL_I
311
SIGNAL_X
321
COMPLEX
MULTIPLEXER
315
Y
323
TRELLIS
CONFIDENCE
SIGNAL
227
ACCUMULATOR
LIMITER
305
DIGITAL
FILTER
307
SIGNAL_Q
313
ERROR
DETECTOR
325
GAIN ERROR 333
341
SIN (Φ)
343
COS (Φ)
TRELLIS
DECISION
SIGNAL
226
SINE/
COSINE
TABLE
317
PHASE
ERROR (Φ)
329
ACCUMULATOR
319

Figure 4

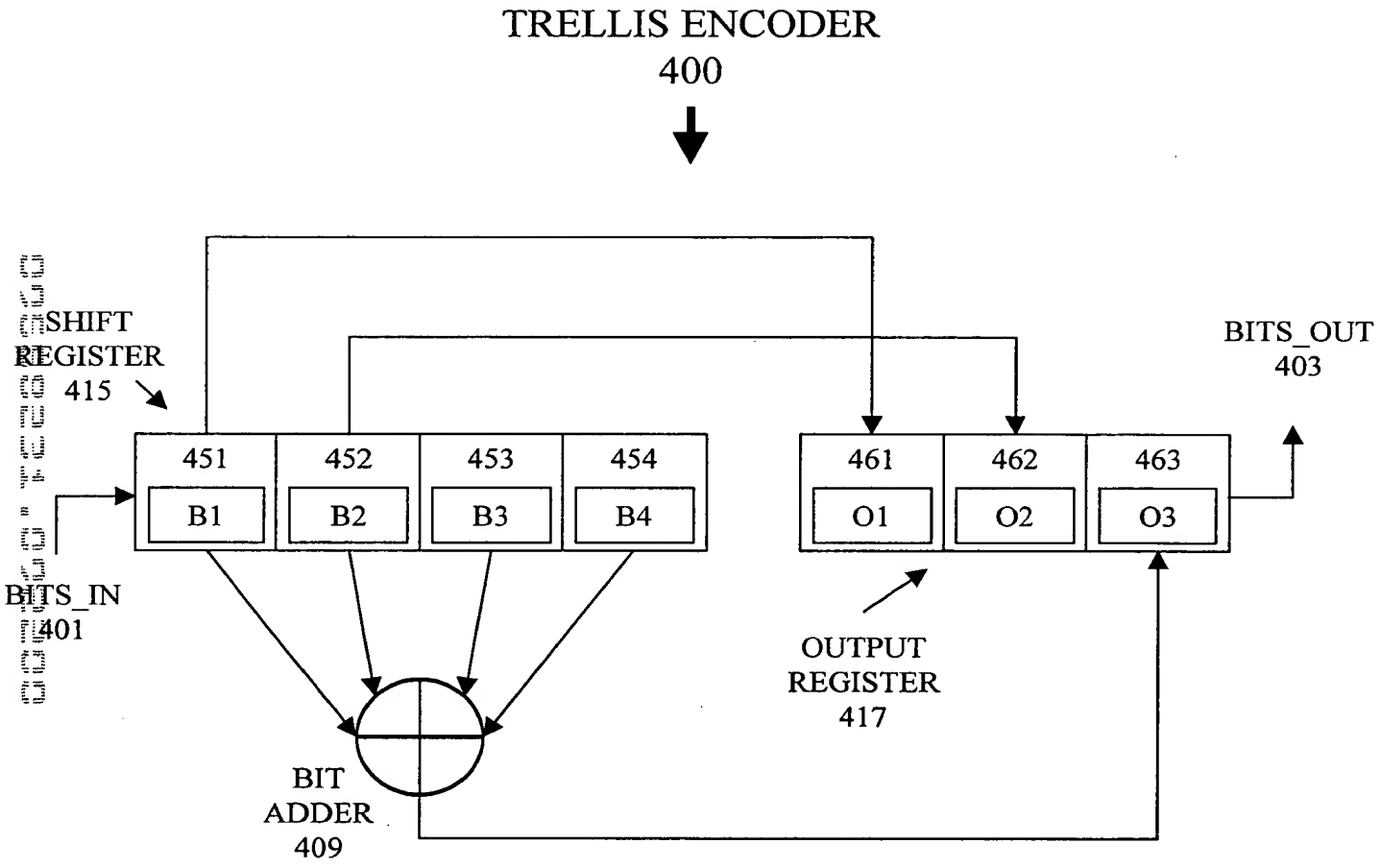

TRELLIS ENCODER
400
SHIFT
REGISTER
415
451
452
453
454
B1
B2
B3
B4
461
462
463
O1
O2
O3
BITS_OUT
403
BITS_IN
401
OUTPUT
REGISTER
417
BIT
ADDER
409

Figure 5

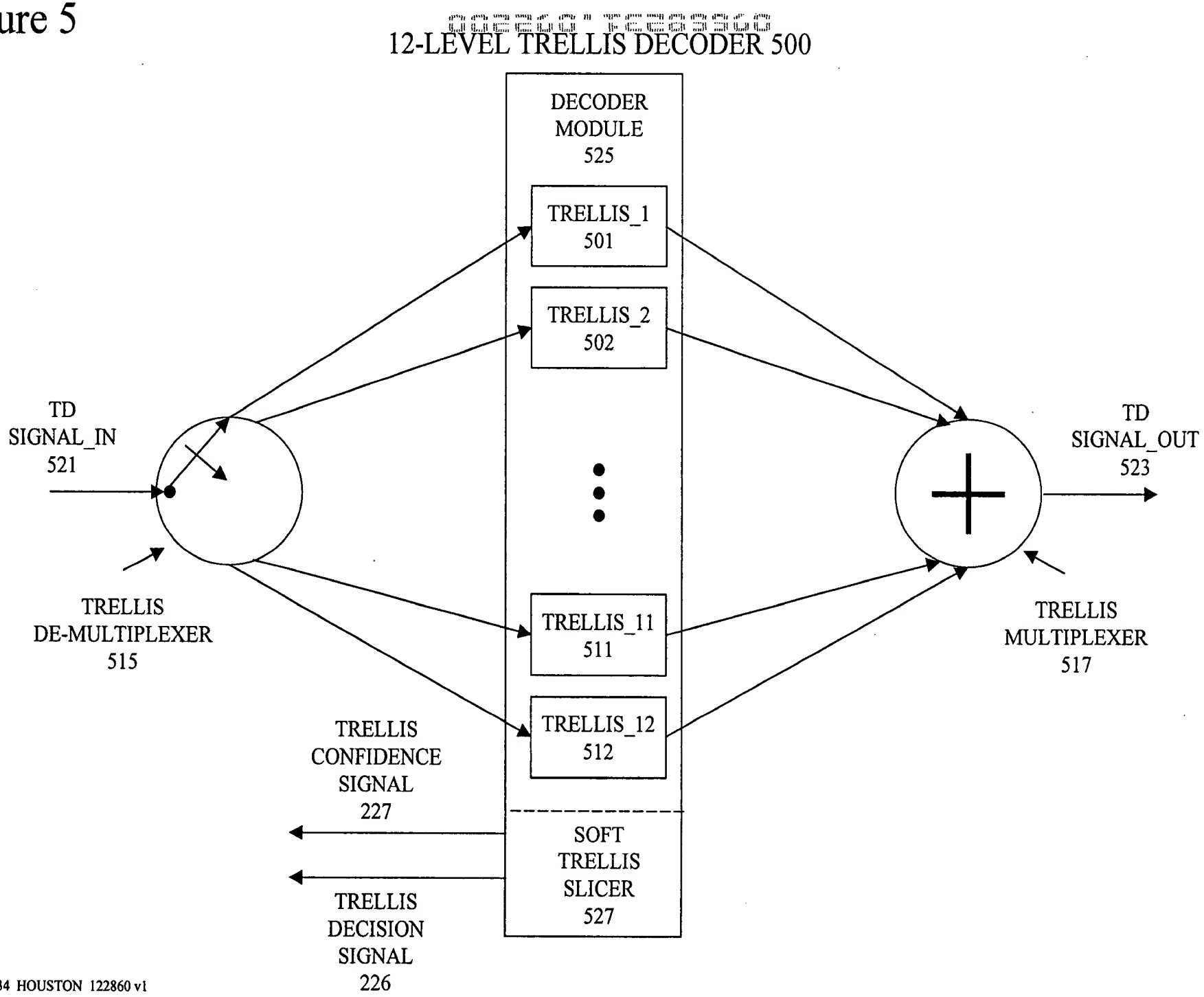
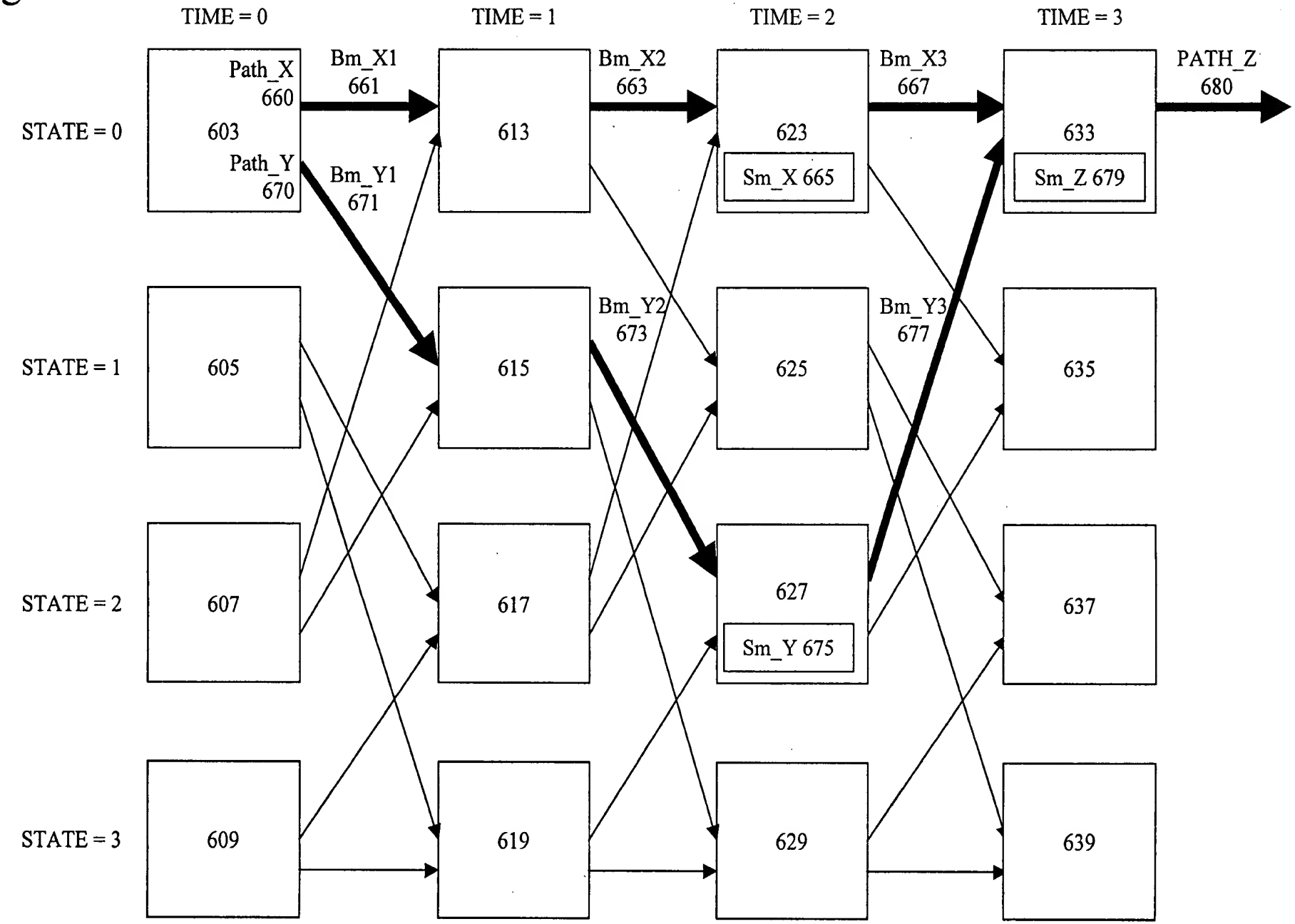

12-LEVEL TRELLIS DECODER 500
DECODER MODULE 525
TRELLIS_1 501
TRELLIS_2 502
TRELLIS_11 511
TRELLIS_12 512
SOFT TRELLIS SLICER 527
TD SIGNAL_IN 521
TRELLIS DE-MULTIPLEXER 515
TRELLIS CONFIDENCE SIGNAL 227
TRELLIS DECISION SIGNAL 226
TD SIGNAL_OUT 523
TRELLIS MULTIPLEXER 517

Figure 6


TIME = 0
TIME = 1
TIME = 2
TIME = 3
STATE = 0
STATE = 1
STATE = 2
STATE = 3
Path_X
660
603
Path_Y
670
Bm_X1
661
Bm_Y1
671
Bm_X2
663
Bm_Y2
673
Bm_X3
667
Bm_Y3
677
PATH_Z
680
613
615
617
619
623
Sm_X 665
625
627
Sm_Y 675
629
633
Sm_Z 679
635
637
639
605
607
609